SPECIFICATION FOR LCD MODULE

Part No.:	MLT021Q20-2
Customer No.:	
Spec Version:	01
Issued Date:	2017-6-21
Customer approval:	

Designed 设计者	Checked 审核者	Approved 核准者

※Please pay more attention for the “inspection standard”, we assume you already agree this standard when place an order with us.

※The specification of “TBD” should refer to the measured value of sample .

Documents Revision History:

Rivision	Date	Description	Changed By
01	2017/6/21	New released	

1. General Description

- The MLT021Q20-2 model is a round Color TFT LCD supplied by Maclight Display Co Ltd.
- This main Module has a 2.1 inch active display area with 320(RGB)X320 resolution. Each pixel is divided into Red, Green and Blue sub-pixels and dots, which are arranged in vertical stripes.
- The MLT021Q20-1 has been designed to apply the MIPI interface method that enables low power, high speed, and high contrast.

2. Mechanical Specification

ITEM	Standard Value	Unit
Display Mode	Normally White, Transmissive LCD	
Module Dimension	57.18(W)*61.97(H)*2.34(T)	mm
Resolution	320(RGB)X 320	Pixels
Active Display Area	Φ 53.38(Diameter)	mm
Pixel Pitch	0.1668×0.1668	mm
Viewing Direction	ALL	--
LED Backlight Color	White	--
Interface	SPI /MIPI	
Input Voltage	IOVCC=1.8,VCC=2.8	V
LCD driver	ST7796H2-G5	

3. Absolute Max Ratings & Electrical Specification

- **Absolute Max Rating**

Item	Min.	Typ	Max	Unit	Remark
Supply Voltage (V_{CC}/IOV_{CC})	-0.3	--	4.6	V	
Input Voltage(VIN)	-0.5		IOVCC+0.5	V	
Storage Temperature	-20		70	℃	
Operating temperature	-30		80	℃	
Humidity(RH)	--		90%(Max60℃)	RH	

Note:

*1) Liquid Crystal driving voltage.

Due to the characteristics of LC Material, this voltage vary with environmental temperature.

*2) Temp.>60℃, Absolute humidity shall be less than 90%RH at 60℃
*3) Temp.≤60℃, 90%RH MAX.
*4) The recommended operating conditions refer to a range in which operation of this product is guaranteed. Should this range is exceeded, the operation cannot be guaranteed even if the values may be without the absolute maximum ratings.

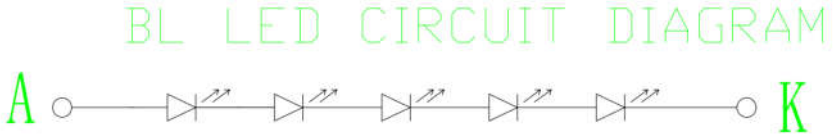
Accordingly, please make sure that the module is used within this range. And these current values are measured under the condition that all devices are stopped, each component is stable and logic signal is input.

■ Electrical Specification

Item	Min.	Typ	Max	Unit	Remark
Supply Voltage for logic (Vcc)	2.6	2.8	3.3	V	
Supply Voltage (IOVcc))	1.7	1.8	3.3	V	
Input Current(I_{DD})	--	15.5	23.3	mA	
Input signal " H"(V_{IH})	0.7*IOVCC	--	IOVCC	V	
Input signal " L"(V_{IL})	GND	--	0.3*IOVCC	V	
Output Voltage ' H ' Level(V_{OH})	0.8IOVCC		IOVCC	V	
Output Voltage ' L ' Level(V_{OL})	GND		0.2IOVCC	V	

■ Backlight Characteristics

Item	Min.	Typ	Max	Unit	Remark
Forward Current(IF)	-	15	-	mA	
Forward Voltage(VF)	12.5	14.5	16.5	V	
Quantity of LED		5		Pieces	



4. Optical Specification

ITEM		SYMBOL	CONDITION	Min.	TYP.	Max.
Color Filter Chromacicity (Note.1)	White	x	θ = ϕ = 0°	0.287	0.307	0.327
		y		0.321	0.341	0.361
		Y		29.0	32.0	35.0
	Red	x	θ = ϕ = 0°	0.633	0.653	0.673
		y		0.312	0.332	0.352
		Y		15.55	18.55	21.55
	Green	x	θ = ϕ = 0°	0.294	0.314	0.334
		y		0.555	0.575	0.595
		Y		58.71	61.71	64.71
	Blue	x	θ = ϕ = 0°	0.117	0.137	0.157
		y		0.113	0.133	0.153
		Y		13.79	15.79	18.79
Transmittance(%) (Note.3)		T	θ = ϕ = 0°	--	5	--

Note.1 These items are measured by C light.
Note.2 Definition of Viewing Angle(θ,ψ),refer to Fig.1 as below：

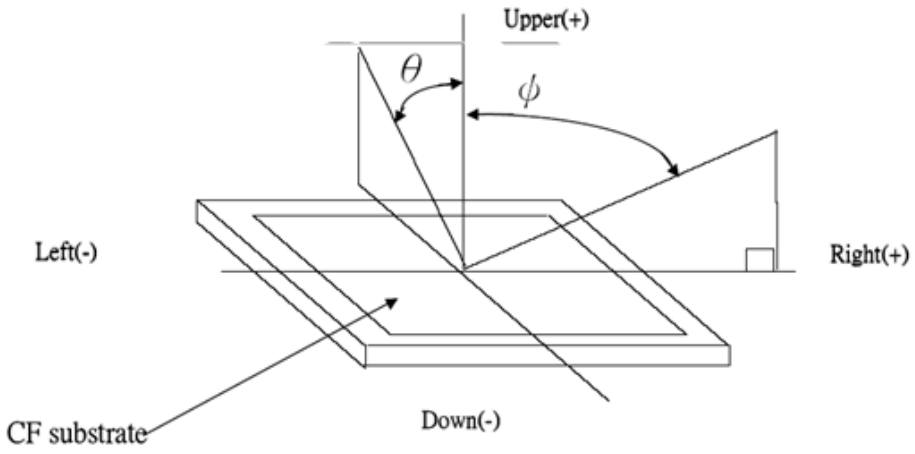
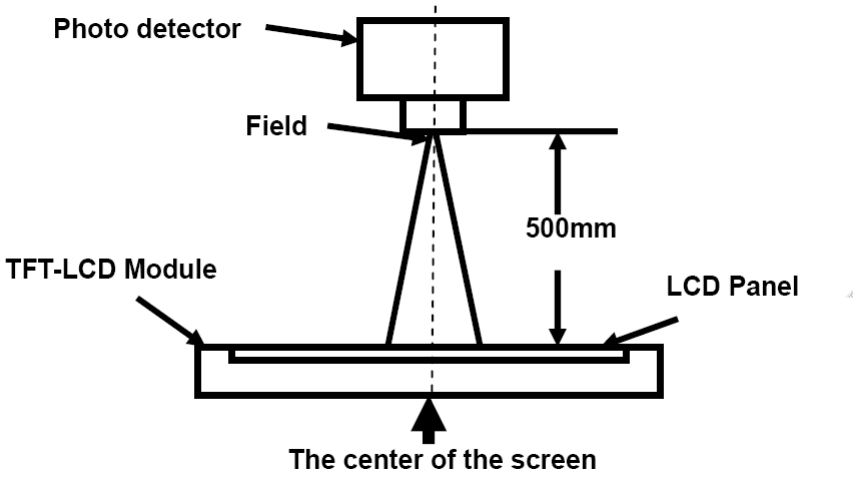


Fig.1 Definition of Viewing Angle

Note.3 Using LC+ EWV Polarizer+Corresponding Backlight, reference only, Measure device：BM-5A (TOPCON)，viewing cone= 1 °，I_L=20mA。

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp	θ=0°	390	480	-	cd/m²	
Uniformity	△Bp	Φ=0°	70	-	-	%	
Viewing Angle	θ1 (Φ=90° or270°)	12 o'clock	-	85	-	Deg	Cr≥10
		6 o'clock	-	85	-		
	θ2 (Φ=0° or 180°)	9 o'clock	-	85	-		
		3 o'clock	-	85	-		
Contrast Ratio	Cr	θ=0° Φ=0°	300	1000		-	
Response Time	t_{on}		-	40	60	ms	
	t_{off}		-			ms	

Electro-optical characteristics test method:



Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined

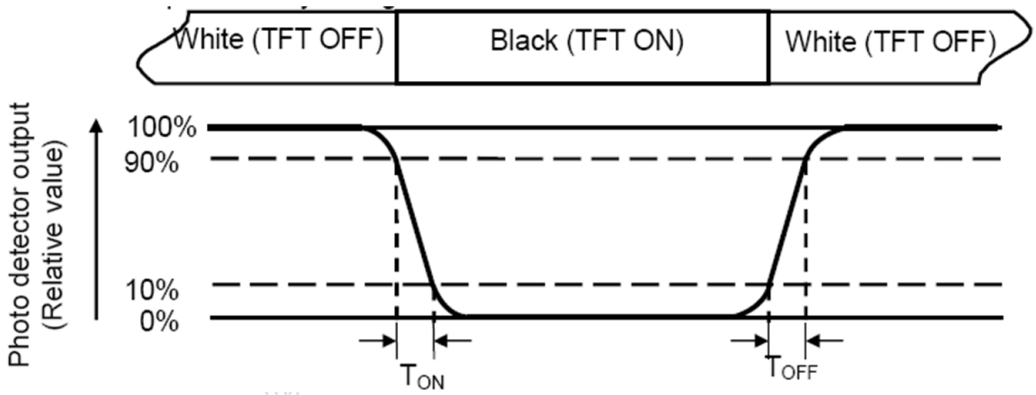
Vblack: To be determined.

Definition of Response Time:

The response time is defined as the LCD optical switching time interval between “White” state and

“Black” state. Rise time (TON) is the time between photo detector output intensity changed from

90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from10% to 90%.



Definition of color chromaticity (CIE1931)

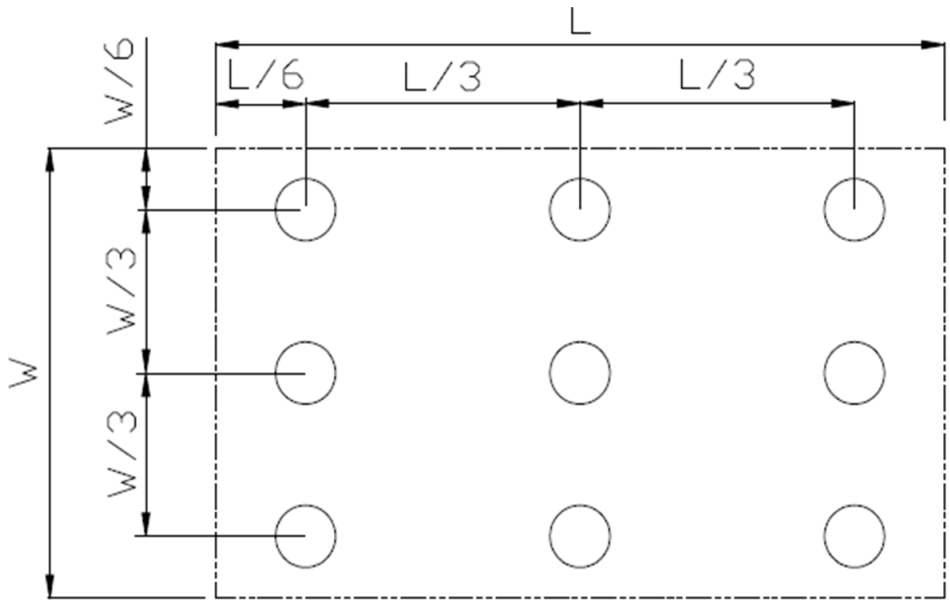
Color coordinates measured at center point of LCD

Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

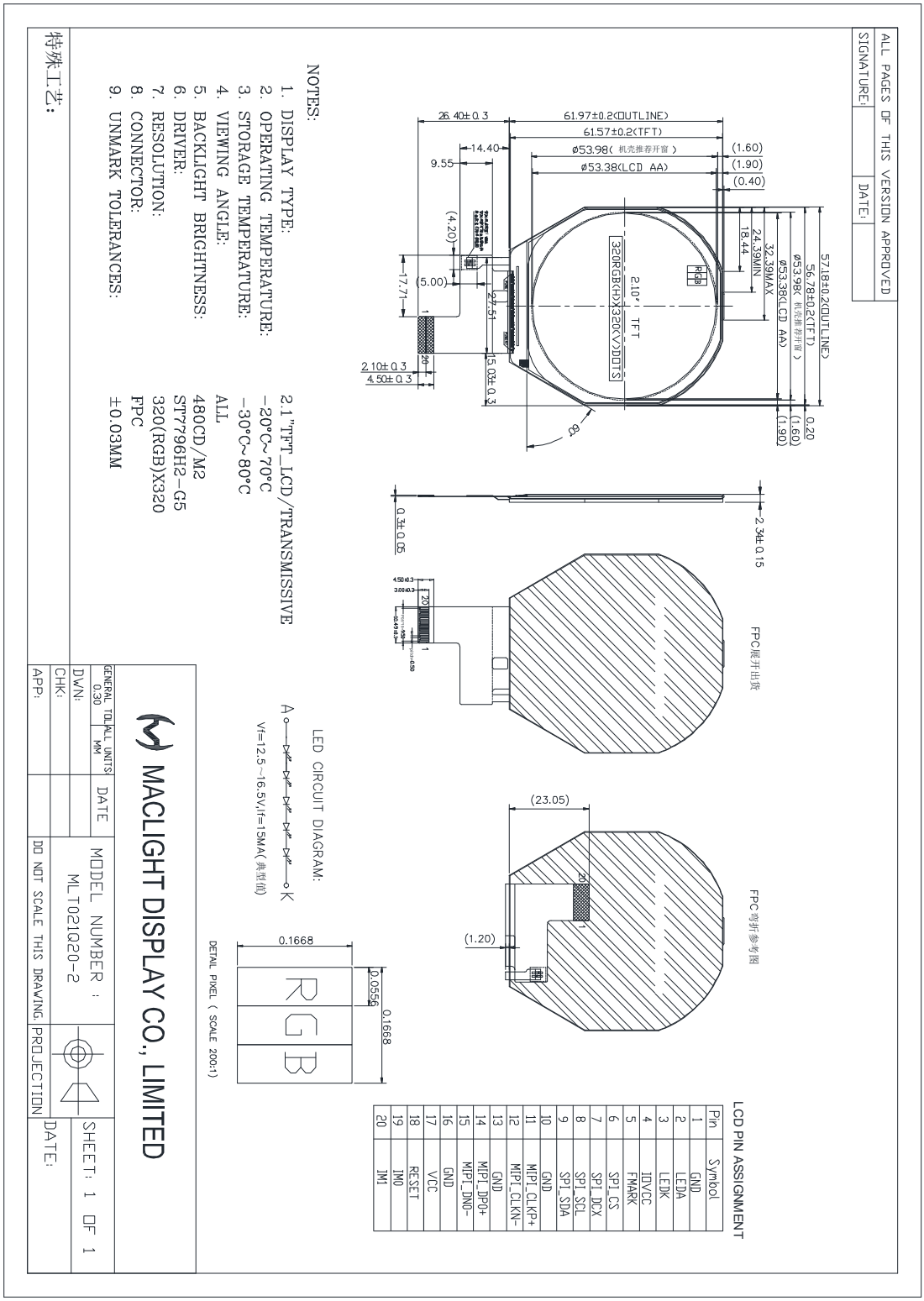
L-------Active area length W----- Active area width



Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position

5. Mechanical Diagram



6. Interface Pin Connections

Interface NO. 接口序号	Symbol 符号	I/O or connect to 输入/出或连接到	Description 描述	When not in use 不用时
1	GND	Power	POWER GROUND	/
2	LEDA	LED driver	LED light Anode	OPEN
3	LEDK	LED driver	LED light Cathode	OPEN
4	IOVCC	Power	Power supply for I/O system.	/
5	FMARK	Out	Tearing effect output	OPEN
6	SPI_CS	In	Chip selection pin.	GND/IOVCC
7	SPI_DCX	In	Display data/command selection pin in SPI interface	GND/IOVCC
8	SPI_SCL	In	Serial input clock	GND/IOVCC
9	SPI_SDA	In/Out	SPI interface input/output pin	GND/IOVCC
10	GND	Power	POWER GROUND	/
11	MIPI_CLKP+	In	Positive polarity of low voltage differential clock signal	OPEN
12	MIPI_CLKN-	In	Negative polarity of low voltage differential clock signal	OPEN
13	GND	Power	POWER GROUND	/
14	MIPI_DP0+	In/Out	Positive polarity of low voltage differential data signal	OPEN
15	MIPI_DN0-	In/Out	Negative polarity of low voltage differential data signal	OPEN
16	GND	Power	POWER GROUND	/
17	VCC	Power	Power supply for analog and booster circuits	OPEN
18	RESET	In	Reset the device	/
19	IM0	In	The interface mode select.	/
20	IM1	In	The interface mode select.	/

-The SPI or MIPI interface mode select.

IM1	IM0	MPU Interface Mode	Data pin
0	0	Reserve	-
0	1	3SPI	SPI_SDA
1	0	MIPI	DN0-/DP0+,CLKN-/CLKP+
1	1	4 Line SPI	SPI_SDA

7. Timing Characteristics

7.1 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.9.

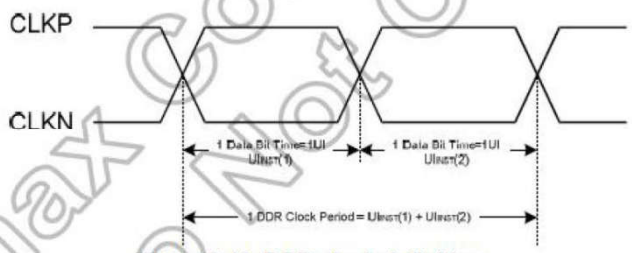


Figure 8.11: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.14.

DSI Mode	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
400Mbps @ 1-lane	UI instantaneous	UI_{INST}	2.5	-	12.5	ns	1, 2

Note: (1) This value 2.5ns corresponds to a maximum 400 Mbps data rate, 12.5ns corresponds to a minimum 80 Mbps data rate
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Table 8.15: Reverse HS data transmission timing parameters

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The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.12. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

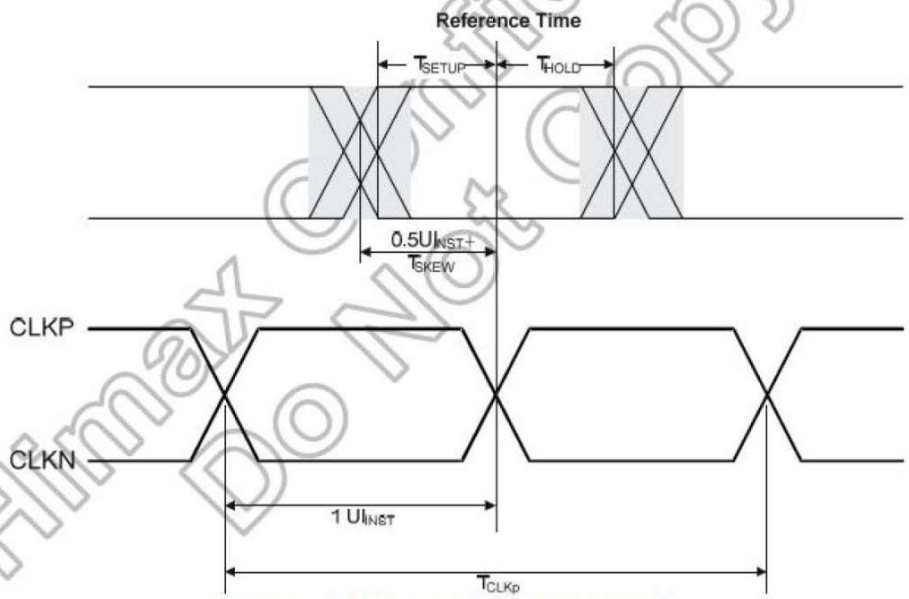

Figure 8.12: Data to clock timing definitions

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7.2 Data-clocl=k Timing Specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UIINST,MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½UIINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15	-	-	UI_{INST}	1
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15	-	-	UI_{INST}	1

Note: (1) Total setup and hold window for receiver of $0.3*UI_{INST}$.

Table 8.16: Data to clock timing specifications

7.3 HS Burst Timing Configuration

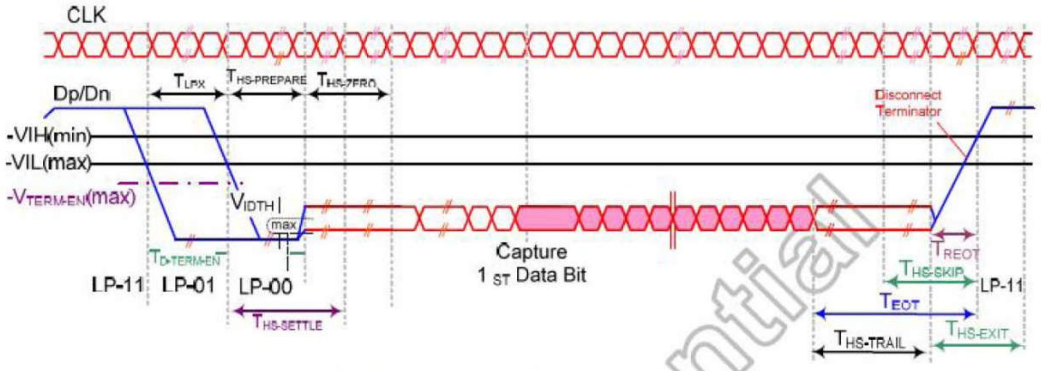

Figure 8.13: High-Speed Data Transmission in Bursts

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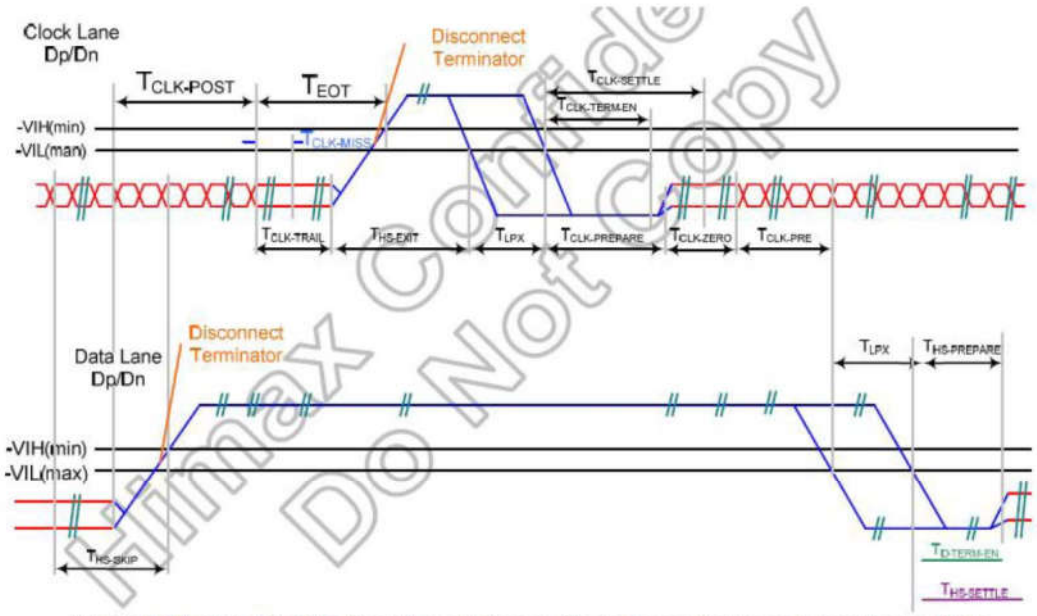

Figure 8.14: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min.	Max.	Unit	Note
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.		60	ns	1,5
$T_{CLK-POST}$	Time that transmitter send HS clock after last associated Data Lane has transitioned to LP Mode.	60ns + 52UI		ns	4
$T_{CLK-PRE}$	Time that HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition form LP to HS mode.	8		UI	4
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95	ns	4
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95	300	ns	5,6
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX}.	Time for Dn to reach $V_{TERM-EN}$	38	ns	5
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		ns	4
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300		ns	4
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	35ns+4UI	ns	5
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.		105ns + 12UI	ns	4
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100		ns	4
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4UI	85ns + 6UI	ns	4

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8. Inspection Standard

A. Sampling Method

Unless otherwise agreed upon in writing, the sampling inspection shall be applied to theCustomer's incoming inspection.

1) Lot size: Quantity per shipment lot
2) Sampling type: Normal inspection , single sampling
3) Inspection level: Ⅱ
4) Sampling table: MIL-STD-105D
5) Acceptable Quality Level(AQL): Major=0.65Minor=1.5

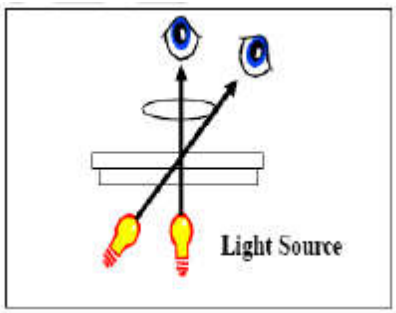
B. Inspection Method

1) Ambient Condition:
   a. Temperature: Room temperature 25±5℃
   b. Illumination: Single fluorescent lamp non-directive(300 to 700 Lux)
2) Viewing distance

The distance between the LCD and the inspector's eyes shall be at least 30-50cm.

3) Viewing Angle

The inspection shall be conducted within normal viewing angle range.



9. Inspection Criteria

1) Major defect

NO.	Item	Inspection Standard	Classification defect
1	All function defect	No display Display abnormal	Major

		Short circuit Missing segment Excess power consumption No backligt, flickering	
2	missing	Missing compement	Major
3	Outline dimension	Outline Dimension out of drawing tolerance	Major

2) Cosmetic defect

A. Definition of inspection range

For dot defect of TFT LCD which is not smaller than 3 inches, dividing three areas to make a judgment (according to figure 1).

A area : center of viewing area

B area : periphery of viewing area

C area : Outside viewing area

For other defects, dividing two areas to make a judgment (according figure 2).

A zone : Inside Viewing area

B zone : Outside Viewing area

X1(A.A~V.A): 2mm X2(A.A~V.A): 2mm

Y1(A.A~V.A): 2mm Y2(A.A~V.A): 2mm

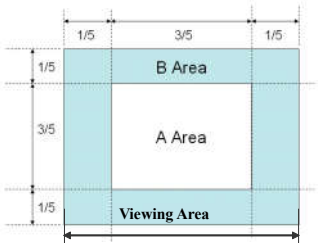


Figure 1

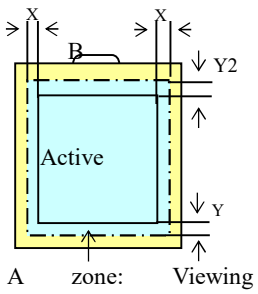


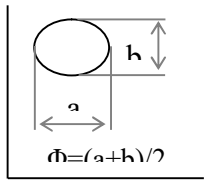
Figure 2

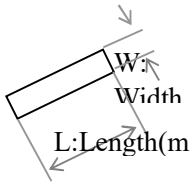
B. Cosmetic defect criteria

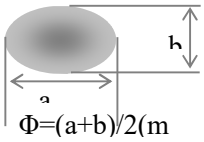
Inspection items	Judgment standard		
	Category	Acceptable number	
		A zone	B zone

<table>
<tr><td rowspan="6">1</td><td rowspan="6">Black spot, White spot, Bright Spot,

Pinhole, Foreign

Particle, Particle in or on glass, Scratch on glass</td><td rowspan="6">  </td><td>A</td><td>Φ≦0.10</td><td>Neglected</td><td rowspan="6">Neglected</td></tr>
<tr><td>B</td><td>0.10<Φ≦0.15</td><td>2</td></tr>
<tr><td>C</td><td>0.15<Φ≦0.20</td><td>1</td></tr>
<tr><td>D</td><td>0.20<Φ</td><td>0</td></tr>
<tr><td colspan="2"></td><td>3</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td></tr>
<tr><td rowspan="6">2</td><td rowspan="6">Black line, White line, and Particle Between

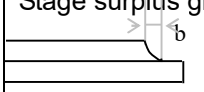
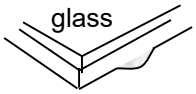
Polarizer and glass, Scratch on glass</td><td rowspan="6">  </td><td>A</td><td>W≦0.01</td><td>Neglected</td><td rowspan="6">Neglected</td></tr>
<tr><td>B</td><td>0.01<W≦0.03 L≦3.0</td><td>2</td></tr>
<tr><td>C</td><td>0.03<W≦0.05 L≦3.0</td><td>1</td></tr>
<tr><td>D</td><td>0.05<W</td><td>0</td></tr>
<tr><td colspan="2"></td><td>3</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td></tr>
<tr><td rowspan="6">3</td><td rowspan="6">Contrast

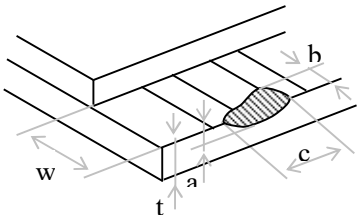
variation</td><td rowspan="6">  </td><td>A</td><td>Φ≦0.2</td><td>Neglected</td><td rowspan="6">Neglected</td></tr>
<tr><td>B</td><td>0.2<Φ≦0.3</td><td>2</td></tr>
<tr><td>C</td><td>0.3<Φ≦0.4</td><td>1</td></tr>
<tr><td>D</td><td>0.4<Φ</td><td>0</td></tr>
<tr><td colspan="2"></td><td>3</td></tr>
<tr><td colspan="2">Total defective point(B,C)</td></tr>
<tr><td rowspan="12">4</td><td rowspan="12">Dot defect (if TFT LCD is used)</td><td rowspan="6">TFT LCD is smaller than 3 inches</td><td>LCD Class</td><td>Defect</td><td colspan="2">A area</td><td>B area</td></tr>
<tr><td rowspan="3">A</td><td>Bright dot</td><td colspan="2">1</td><td rowspan="6">Neglected</td></tr>
<tr><td>Dark dot</td><td colspan="2">2</td></tr>
<tr><td>Total</td><td colspan="2">2</td></tr>
<tr><td rowspan="3">B</td><td>Bright dot</td><td colspan="2">2</td></tr>
<tr><td>Dark dot</td><td colspan="2">3</td></tr>
<tr><td>Total</td><td colspan="2">4</td></tr>
<tr><td rowspan="6">TFT LCD between 3~10.4 inches</td><td>LCD Class</td><td>Defect</td><td>A area</td><td>B area</td><td>C area</td></tr>
<tr><td rowspan="3">A</td><td>Bright dot</td><td>1</td><td>1</td><td rowspan="6">Neglected</td></tr>
<tr><td>Dark dot</td><td>1</td><td>2</td></tr>
<tr><td>Total</td><td colspan="2">4</td></tr>
<tr><td rowspan="3">B</td><td>Bright dot</td><td>2</td><td>2</td></tr>
<tr><td>Dark dot</td><td>2</td><td>3</td></tr>
<tr><td>Total</td><td colspan="2">6</td></tr>
<tr><td colspan="5">Notes:

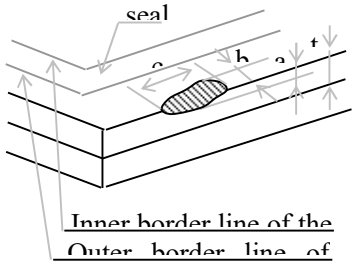
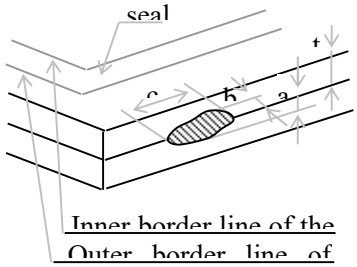
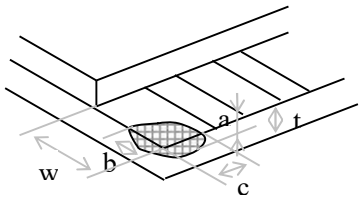
Bright dot: in R、G、B or dark display figure, the pixel appears bright.

Dark dot: in R、G、B or white display figure, the pixel appears dark.

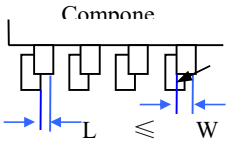
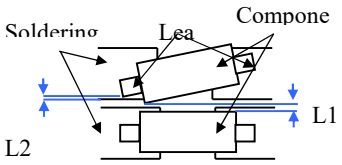
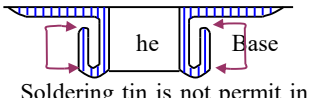
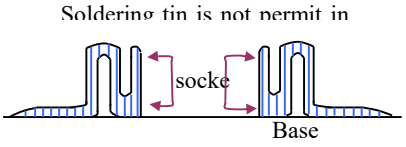
Defect area must be less than an half size of the dot.</td></tr>
<tr><td>5</td><td colspan="2">Bubble inside cell</td><td colspan="2">any size</td><td>none</td><td>none</td></tr>
</table>

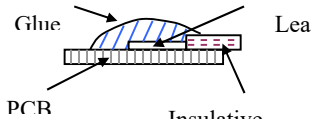
6	Polarizer defect (if Polarizer is used)	Scratch ,damage on polarizer, Particle on polarizer or between polarizer and glass.	Refer to item 1 and item 2.			
		Bubble, dent and convex	A	Φ≦0.3	Neglected	Neglected
			B	0.3<Φ≦0.7	2	
			C	0.7<Φ	0	
7	Surplus glass	Stage surplus glass 	b≦0.3mm			
		Surrounding surplus glass 	Should not influence outline dimension and assembling.			
11	Contrast ratio uneven		According to the limit specimen			
12	Crosstalk		According to the limit specimen			
13	Black /White spot(display)		Refer to item 1			
14	Black /White line(display)		Refer to item 2			

Inspection items			Judgment standard		
			Category(application: B zone)		Acceptable number
15	Glass defect crack	①The front of lead terminals 	A	a≤ t, b≤1/5W, c≤3mm	Max.3 defects allowed
			B	Crack at two sides of lead terminals should not cover patterns and alignment mark	

		②Surrounding crack—non-contact side 		b < Inner borderline of the seal	
		③ Surrounding crack— contact side 		b < Outer borderline of the seal	
		④Corner 	A	a ≦ t, b ≦ 3.0, c ≦ 3.0	
			B	Glass crack should not cover patterns u and alignment mark and patterns.	

Inspection items	Judgment standard
	Category(application: B zone)

16	PCB defect	Component soldering: No cold soldering、short、open circuit、burr、tin ball The flat encapsulation component position deviation must be less than 1/3 width of the pin (Pic.1)； the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted（Pic.2）	 
		lead defect: The lead lack must be less than 1/3 of its width; The lead burr must be less than 1/3 of the seam; Impurities connect with the near leads is not permitted	
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted	 

		Glue on root of the speaker receiver and motor lead: The insulative coat of the lead must join into the PCB; the protected glue must envelop to the insulative coat.	

10. Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.2.4 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.